REMARKS

Applicants file concurrently herewith the Petition and Fee for Extension of Time pursuant to 37 C.F.R. § 1.136.

Applicants thank the Examiner for considering the reference provided with the Information Disclosure Statement (paper no. 4) filed on August 30, 2001.

The drawings have been objected to and claims 11 and 16 have been rejected under 35 U.S.C. § 112 (first paragraph) on the ground that the drawings did not illustrate a through hole in the metal plate. New drawings, Figs. 11A-11C, are provided to illustrate the through holes. A description of the through holes is provided at page 26, lines 1-4 and thus the new drawings are supported by the specification as originally filed and no new matter has been added. Approval of the drawings and withdrawal of the 35 U.S.C. § 112 (first paragraph) rejection, which is traversed as the specification as originally filed contains disclosure of the through holes, are respectfully requested.

The title of the invention has been objected to. A new title more descriptive of the invention is submitted herewith. Approval of the new title is respectfully requested.

Claim 8 has been rejected under 35 U.S.C. § 112 (second paragraph) on the ground that the word "concave" is not commonly used in semiconductor technology. Claim 8 has been amended as suggested by the Examiner to replace the word "concave" with the term "stepped part". The scope of the claim remains the same with this amendment. Withdrawal of the 35 U.S.C. § 112 (second paragraph) rejection is requested.

Claims 1-20 have been examined. Claims 18-20 have been cancelled without disclaimer or prejudice and have been replaced by new claims 21-27 to more fully claim applicants' invention. Thus, claims 1-17 and claims 21-27 remain in this application.

Applicants thank the Examiner for indicating the claims 4-6, 12 and 17 contain allowable subject matter and would be allowed when written in independent form. Claim 4 has been written in independent form to include the limitations of claims 1, 2 and 3. Claim 12 has been written in independent form to include the limitations of claims 1 and 8. Claim 17 has been written in independent form the include the limitations of claims 1 and 13. Thus, independent claims 4, 12, and 17 are now in condition for allowance based on the Examiner's prior indication of allowance with respect to those claims.

Claims 1-3, 7 and 18 have been rejected under 35 U.S.C. § 102(b) as anticipated by Williams et al. (United States Patent No. 6,307,755). Claim 1 is independent. Claims 2-3 and 7 depend from claim 1.

Williams et al. discloses a semiconductor device having a die 462, a bottom lead frame 470, and a copper strap 460 connecting the die 462 to the bottom lead frame 470 as shown in FIG. 19O. The copper strap 460 is a camel hump piece of metal, as described in column 18, lines 46-56. However, Williams et al. does not disclose that the copper strap 460 has any roughened surface opposed to a surface which is joined to the die 462. Therefore, Williams et al. merely discloses the prior art also disclosed in the specification of the present application.

On the other hand, a semiconductor device according to the presently rejected claims of the present invention has a metal plate having a first main surface joined to lead terminals and a

second main surface opposed to the first main surface. The second main surface is roughened to have a plurality of recesses, which are filled with a molding resin sealing a semiconductor chip. Thus, adhesion strength between the metal plate and the molding resin is improved to prevent the molding resin from separating from the metal plate even under severe environments in which the temperature, the humidity, and the pressure are fluctuated. As a result, the semiconductor device according to the present invention prevents impurities causing corrosion of the semiconductor chip, such as water, gas, or the like, from penetrating into the semiconductor device through any separation between the metal plate and the molding resin. This to improves reliability.

In view of the foregoing, it is respectfully submitted that claims 1-3 and 7 patentably distinguish over Williams et al. It is further submitted that new claims 21-27 patentably distinguish over Williams et al. at least for the reasons given above with respect to claims 1-3 and 7.

Claim 8, which depends from claim 1, is rejected under 35 U.S.C. § 103(a) as unpatentable over Williams et al. in view of Kuraishi et al. (United States Patent No. 5,859,471). This rejection is respectfully traversed. Claim 8 distinguishes over Williams et al. for at least the reasons set forth above with respect to claim 1. It is respectfully submitted that the Kuraishi et al. reference fails to make up the deficiencies of the Williams et al. reference. Clearly Kuraishi et al. neither discloses nor suggests the foregoing distinctions between applicants' claimed invention and the William et al. reference.

Claims 9, 10, 13, 14, and 15, which are dependent upon claim 8, are rejected under 35 U.S.C. § 103 as unpatentable over Williams et al. in view of Kuraishi et al. and further in view of

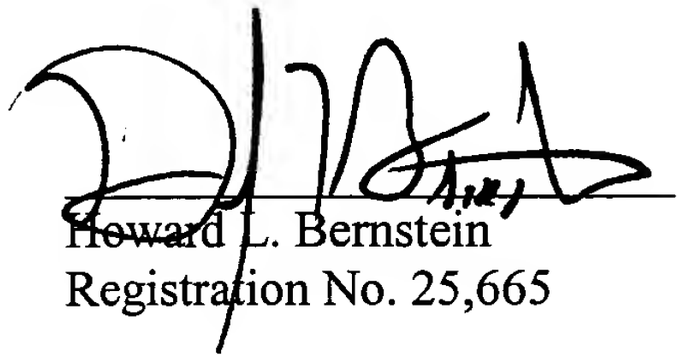
Seki et al. (United States Patent No. 6,165,819). This rejection is respectfully traversed. Claims 9, 10, 13, 14 and 15 patentably distinguish over Williams and Kuraishi et al. for at least the reasons set forth above with respect to claims 1 and 8. Seki et al. fails to make up the deficiencies of Williams et al. and Kuraishi et al. Seki et al. clearly fails to disclose or suggest the distinguishing features between applicants' invention as claimed in claim 1 and Williams et al. as set forth above with respect to claim 1. Withdrawal of this rejection is also respectfully requested.

In view of the foregoing, it is respectfully submitted that claims 1-3, 5-11, 13-17, and 21-27 patentably distinguish over Williams et al., Kuraishi et al. and Seki et al., taking individually or in combination and therefore these claims are now patentable and the application in condition for allowance.

It is therefore requested that the application be passed to issue at the earliest possible time. If for any reason the Examiner finds the application other than in condition for allowance. he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 293-7060 to discuss the steps necessary for placing the application in condition for allowance

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: October 8, 2002

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title is changed as follows:

SEMICONDUCTOR DEVICE WITH UNEVEN METAL PLATE TO IMPROVE ADHESION TO MOLDING COMPOUND

IN THE SPECIFICATION:

The specification is changed as follows:

Page 21, second full paragraph:

FIGS. 9A and 9B are illustrations showing the semiconductor device 4 of the embodiment 2 of the present invention, FIG. 9A is a plane view and FIG. 9B is a cross-section cut along the line VIII-VIII' of FIG. 9A; [and]

Page 21, third full paragraph:

FIGS. 10A to 10D are illustrations showing the copper plate 56 to be employed for the semiconductor device 4 of the embodiment 2 of the present invention. FIG. 10A is a plane view, FIG. 10B is a cross-section cut along the line IX-IX' of FIG. 10A, FIG. 10C is a bottom face of FIG. 10B, and FIG. 10D is a cross-section cut along the line X-X' of FIG. 10A; and

FIGS. 11A to 11C are illustrations showing the copper plate 51 (example 1) to be employed for the semiconductor device 3 of the embodiment 1 of the present invention. FIG.

11A is a plane view, FIG. 11B is a cross-section cut along the line XI-XI' of FIG. 11A, and FIG. 11C is a bottom face of FIG. 11B.

Page 25, last paragraph (which bridges over to page 26):

As illustrated in FIGS. 4A and 4B, the copper plate 51 has dimples 53 in the upper face. The dimples 53 are those formed in the copper plate 51 and can be formed by etching and pressing. In the case of forming them by etching, they are formed by half etching, which is incompletely carried out etching. In the case where etching is completely carried out, the amount of copper removed is increased and the resistance value of the copper plate 51 is increased. In the case where the copper plate 51 has nothing to do with the resistance value, etching may completely be carried out and through holes may be formed instead of the dimples 53. That is because the adhesion strength to the molding resin 8 can be improved by through holes. The copper plate 51 having through holes 59 is shown in FIGS. 11A to 11C. Through holes 59 are formed instead of the dimples 53 of FIGS. 4A and 4B.

IN THE CLAIMS:

Claims 18-20 are canceled.

The claims are amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;

wiring materials having a plurality of lead terminals elongated in a first direction;

a metal plate having a first main surface and a second main surface opposed to said first main surface, wherein said metal plate is joined to[connecting with] said plurality of electrodes at a first end portion of said first main surface[metal plate] and is joined to[connecting with] said plurality of lead terminals at a second end portion of said first main surface facing to said first end portion[metal plate] to connect said plurality of electrodes and said plurality of lead terminals; and

a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein

said second main[a] surface of said metal plate is roughened, said second main surface having a plurality of recesses filled with said molding resin[uneven and joined to said molding resin].

2. (Amended) The semiconductor device as claimed in claim 1, wherein said metal plate connects with said plurality of electrodes and said plurality of lead terminals by a plating formed on said first main surface[metal plate].

3. (Amended) The semiconductor device as claimed in claim 2, wherein said metal plate has at least one bent part elongated in a second direction crossing said first direction between said first end portion and said second end portion, and

wherein said plating is formed on said first end portion and said second end portion.

4. (Amended) [The semiconductor device as claimed in claim 3]A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;

wiring materials having a plurality of lead terminals;

a metal plate connecting with said plurality of electrodes at a first portion of said metal plate and connecting with said plurality of lead terminals at a second portion of said metal plate;

a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein

a surface of said metal plate is uneven and joined to said molding resin;

wherein said metal plate connects with said plurality of electrodes and said plurality of lead terminals by a plating formed on said metal plate;

wherein said metal plate has at least one bent part between said first portion and said second portion; and

wherein said plating is formed only on said first portion and said second portion.

8. (Amended) The semiconductor device as claimed in claim 3, wherein said plurality of lead terminals have a stepped part[concave], and

wherein said metal plate are connected with said stepped part[concave] by a conductive bonding material.

9. (Amended) The semiconductor device as claimed in claim 8, wherein said roughened second main surface of said metal plate is [roughened]a sand blasted surface.

10. (Amended) The semiconductor device as claimed in claim 8, wherein said second main surface of said metal plate is dimpled.

12. (Amended) [The semiconductor device as claimed in claim 8]A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;

wiring materials having a plurality of lead terminals;

a metal plate connecting with said plurality of electrodes at a first portion of said metal plate and connecting with said plurality of lead terminals at a second portion of said metal plate;

a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein

a surface of said metal plate is uneven and joined to said molding resin;

wherein said plurality of lead terminals have a stepped part; and

wherein said metal plate is connected with said stepped part by a conductive bonding material; and

wherein said surface of said metal plate has a plurality of whisker platings.

13. (Amended) The semiconductor device as claimed in claim 3, wherein said metal plate has claw parts being extended from an edge part of said metal plate and being fitted in intervals of two of said wiring materials.

14. (Amended) The semiconductor device as claimed in claim 13, wherein said roughened second main surface of said metal plate is [roughened]a sand blasted surface.

15. (Amended) The semiconductor device as claimed in claim 13, wherein said second main surface of said metal plate is dimpled.

17. (Amended) [The semiconductor device as claimed in claim 13]A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;

wiring materials having a plurality of lead terminals;

a metal plate connecting with said plurality of electrodes at a first portion of said metal plate and connecting with said plurality of lead terminals at a second portion of said metal plate;

a molding resin sealing said semiconductor chip, parts of said wiring materials, and said metal plate, wherein

a surface of said metal plate is uneven and joined to said molding resin;

wherein said metal plate has claw parts fitted in said wiring materials; and

wherein said surface of said metal plate has a plurality of whisker platings.

Claims 21-27 are added as new claims.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoshihiro NAKAJIMA, et al.

Appln. No.: 09/941,744

Confirmation No.: 7388

Filed: August 30, 2001

For: SEMICONDUCTOR DEVICE

Docket No: Q64096

Group Art Unit: 2826

Examiner: Pershelle L. GREENE

EXCESS CLAIM FEE PAYMENT LETTER

Commissioner for Patents
Washington, D.C. 20231

Sir:

An Amendment Under 37 C.F.R. § 1.111 is attached hereto for concurrent filing in the above-identified application. The resulting excess claim fee has been calculated as shown below:

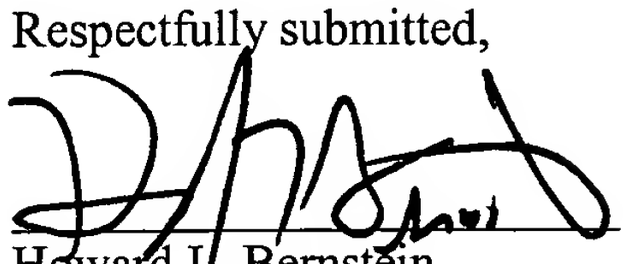
	After Amendment		Highest No. Previously Paid For				
All Claims	24	- 20	= 4	X	$18.00	=	$72.00
Independent	5	- 3	= 2	X	$84.00	=	$168.00
			TOTAL			=	**$240.00**

A check for the statutory fee of $240.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to

Excess Claim Fee Payment Letter
Application NO. 09/941,744

Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this letter is enclosed.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: October 8, 2002

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Yoshihiro NAKAJIMA, et al.

Appln. No.: 09/941,744

Confirmation No.: 7388

Filed: August 30, 2001

Docket No: Q64096

Group Art Unit: 2826

Examiner: Pershelle L. GREENE

For: SEMICONDUCTOR DEVICE

EXCESS CLAIM FEE PAYMENT LETTER

Commissioner for Patents
Washington, D.C. 20231

Sir:

An Amendment Under 37 C.F.R. § 1.111 is attached hereto for concurrent filing in the above-identified application. The resulting excess claim fee has been calculated as shown below:

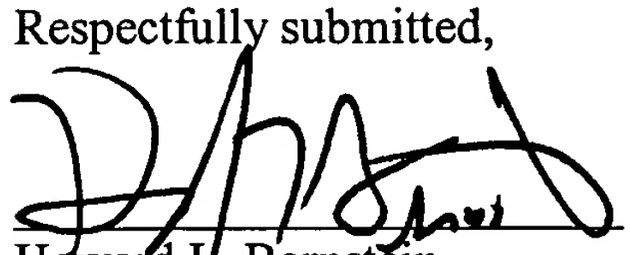
	After Amendment		Highest No. Previously Paid For				
All Claims	24	-	20	=	4	X $18.00	= $72.00
Independent	5	-	3	=	2	X $84.00	= $168.00
					TOTAL		= **$240.00**

A check for the statutory fee of $240.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to

Excess Claim Fee Payment Letter
Application NO. 09/941,744

Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this letter is enclosed.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: October 8, 2002